Rubén Salvador | Associate Professor

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MDXHoWoAAAAJ

Research Interests

My research interests span the areas of **embedded computing architectures, reconfigurable computing, hardware security and self-adaptive systems**. I work on building reconfigurable architectures for adaptive hardware, designing and programming novel accelerator architectures, and digging around with hardware security. Recently, I have started working on hardware security for machine learning, specifically on side-channel attacks resistant implementations of DNN/CNN hardware accelerators. Overall, my research work aims at building more efficient, secure, and intelligent systems.

Positions and career

Appointments

2019–today **Associate Professor**, *CentraleSupélec*, Rennes, France
Associate researcher at IETR Lab, *Institut d'Electronique et des Technologies du numéRique*

2017–2019 **Assistant Professor**, *Universidad Politécnica de Madrid*, Madrid, Spain
Telecommunications Systems Engineering School (ETSIST)
Research Center on Software Technologies and Multimedia Systems (CITSEM)

2012–2017 **Teaching Assistant**, *Universidad Politécnica de Madrid*, Madrid, Spain
Telecommunications Systems Engineering School (ETSIST)
Research Center on Software Technologies and Multimedia Systems (CITSEM)

2008–2011 **PhD Researcher**, *Universidad Politécnica de Madrid*, Madrid, Spain
Industrial Engineering School (ETSII)
Center of Industrial Electronics (CEI)

2006–2007 **Research Engineer**, *Universidad Politécnica de Madrid*, Madrid, Spain
Center of Industrial Electronics (CEI)

2005–2006 **Research Engineer**, *Universidad Politécnica de Madrid*, Madrid, Spain
University Institute for Automobile Research (INSIA)

Visiting positions

2017 **Visiting Professor**, *IETR/INSA Rennes, VAADER team*, Rennes, France, 5 months

2009 **Visiting PhD Student**, *Brno University of Technology*, Brno, Czech Republic, 4 months

Accreditations/Qualifications

2019 **Maître de Conférences (Associate Professor)**, *CNU sections 61 & 63*, France

2016 **Assistant Professor**, Spain

Memberships

2017 **IEEE Member**

2017 **ACM Member**

Education

2015 **Ph.D., Industrial Electronics**, *Universidad Politécnica de Madrid*
"Parametric and structural self-adaptation of embedded systems using evolvable hardware". Supervisors: Eduardo de la Torre (UPM), Lukas Sekanina (Brno Univ. Technology)

2007 **M.Sc. Industrial Electronics**, *Universidad Politécnica de Madrid*
"Embedded intelligence on chip"

2004 **M.Eng. Electronics Engineering**, *Universidad de Alcalá de Henares*
"Research and development of a system for the implementation of audiometric calibration procedures"

2001 **B.Eng. Telecommunications Engineering**, *Universidad Politécnica de Madrid*
"Implementation of narrow-band noise generation algorithms according to ANSI S3.6 1996"

Academic responsibilities

University service

2016–2019 **School Board**, *elected member*, Telecommunications Systems Engineering Schoo, UPM

2014–2015, 2015–2019 **Department Board**, *elected member, member*, Telematics and Electronics Department, UPM

2007–2011 **Research Center Board**, *elected member (non-PhD researchers)*, Center of Industrial Electronics, UPM

Research grants

2021–2024 **ATTILA: Addressing securiTy Threats to artIficiaL intelligence in Approximate computing systems**, *ANR JCJC (young researchers grant)*, PI, 287k€

2021 **Secure Intelligent Systems Lab**, *AIS scientific installation (lab equipment), Rennes Métropole*, PI, 40k€

2021–2024 **Efficient designs of on-board heterogeneous embedded systems for space applications**, *CNES PhD*, co-PI with O. Sentieys and A. Kritikakou, half PhD scholarship

2021 **Side-channel attacks to AI**, *PEPS IETR* (MSc Intern.), PI with M. Mendez-Real, 3.6k€

2021 **Machine Learning for physical layer security in IoT devices**, *PEPS IETR* (MSc Internship), co-PI with J.C. Prévotet (PI), 3.6k€

2020-2023 **SGaLeaks. The Screaming Gate Array: Study and characterization of IP data leakages in mixed-signal FPGA SoCs**, *PEC PhD thesis*, PI with M. Pelcat and A. Nafkha

2020 **Circuit Diversification for Improved Security of FPGA Computing Architectures**, *PEPS IETR* (MSc Internship), PI with M. Pelcat and A. Nafkha, 3.5k€

2017 **Heterogeneous acceleration of Parameterized & Interfaced Synchronous Dataflow (PiSDF) applications**, *HiPEAC collaboration grant*, Visit to IETR/INSA Rennes, 5k€

2017 **Heterogeneous acceleration of Parameterized & Interfaced Synchronous Dataflow (PiSDF) applications**, *INSA Rennes Invited Professor grant*, 3.6k€

2009 **Evolvable hardware applied to adaptive Discrete Wavelet Transforms for image compression in embedded systems**, *UPM*, PhD student visiting grant to Brno Univ. of Technology, 5.5k€ + travel expenses

Research donations

- **Xilinx.** ZCU102 Zynq UltraScale+ Dev. Kit, and other FPGA boards, ~$4000, 2020
- **Intel FPGA.** Intel Arria 10 SoC Dev. Kit, $4495, 2017

Awards

2018 **UPM Innovatech award**, *UPM*, 1st prize, 6th edition
Technological Innovation Workshop. 1st award to 2018 most innovative UPM technology, as part of GDEM team for our work on real-time brain cancer detection using hyperspectral image classification

2016 **Best demo award**, *Best DASIP Demo Night Award*, DASIP 2016
Demo: HELICoiD Tool Demonstrator for Real-Time Brain Cancer Detection

Awards to my students

2018 **Jaime Sancho**, *UPM*, 1st prize, ETSIST MSc thesis poster contest "My project at a glance"
"Energy and Performance Modeling of NVIDIA TX1 Embedded GPU in Hyperspectral Image Classification Tasks for Cancer Detection Using Machine Learning Techniques", UPM

2013 **Iván Flores**, *UPM*, Best MEng thesis award
"Implementation of evolvable hardware in a systolic array by means of virtual reconfigurable circuits", Foundation for the Promotion of Industrial Innovation (`http://www.f2i2.net/`)

Service

Editorial activities

2022– **IEEE Embedded Systems Letters (ESL)**, *Associate Editor*

Conference chairing

2022 **LASCAS**, Latin American Symp. on Circuits and Systems, Track 8 co-chair: Signal, Image and Video Processing

2019 **ACM Computing Frontiers**, Poster session co-chair

2018 **ACM Computing Frontiers**, Short papers & poster session chair

Conference Organizing Committees

2019, 2018 **ACM Computing Frontiers**

Program Committees

2022 **ISVLSI**, IEEE Computer Society Annual Symposium on VLSI, *System Design and Security (SDS) Track*

2022 **PARMA-DITAM**, Workshop on Parallel Programming and Run-Time Management Techniques for Many-core Architectures - Workshop on Design Tools and Architectures for Multicore Embedded Computing Platforms

2022 **LASCAS**, Latin American Symp. on Circuits and Systems

2019– **SAMOS**, Int. Conf. Embedded Computer Systems: Architectures, Modeling And Simulation

2019– **RAPIDO**, Workshop on Rapid Simulation and Performance Evaluation: Methods and Tools

2018– **Computing Frontiers**, ACM Int. Conf. on Computing Frontiers

2017– **CPSWS**, CPS Summer School and Workshop

2017– **ReCoSoC**, Int. Symp. on Reconfigurable Communication-centric Systems-on-Chip

2017– **DASIP**, Conf. on Design and Architectures for Signal and Image Processing

2017– **DCIS**, Conf. on Design of Circuits and Integrated Systems

2014, 2018 **TAEE**, Tecnología, Aprendizaje y Enseñanza de la Electrónica

2013 **SPIE Microtechnologies**, VLSI Circuits and Systems VI

Special sessions, workshops & tutorials

2017 **ReCoSoC**, *High Level Design Methodologies for Reconfigurable Computing and Adaptive Systems: Tool Flows and Applications*, with J. Sérot and E. Juárez

2017 **DASIP**, *Real-time Hyperspectral Image and Video Processing*, with E. Juárez and G. M. Callicó

Reviewing activities

Journals

2021– **JETC**, ACM Journal on Emerging Technologies in Computing Systems

2021– **TCAS-II**, IEEE Transactions on Circuits and Systems II

2020– **FGCS**, Future Generation Computer Systems

2020– **IEEE ESL**, Embedded Systems Letters

2020– **IJPP**, International Journal of Parallel Programming

2018– **TRETS**, ACM Trans.on Reconfigurable Technology and Systems

2018– **JSPS**, Journal of Signal Processing Systems

2017– **JSA**, Journal of Systems Architecture

2017– **IEEE Access**

2017– **IEEE TVLSI**, IEEE Trans. on VLSI Systems

2014– **MICPRO**, Microprocessors and Microsystems

2017– **Integration**, the VLSI Journal

2016– **GENP**, Genetic Programming and Evolvable Machines

2016 **MDPI Computers**

2016 **IET Electronic Letters**

2015 **CJA**, Chinese Journal of Aeronautics

2013 **AEÜ**, Int. Journal of Electronics and Communications

Conferences

2022 **ISVLSI**, IEEE Computer Society Annual Symp. on VLSI

2022 **PARMA-DITAM**, Workshop on Parallel Programming and Run-Time Management Techniques for Many-core Architectures - Workshop on Design Tools and Architectures for Multicore Embedded Computing Platforms

2021– **ISCAS**, International Symposium on Circuits and Systems

2021 **ICCAD**, Int. Conf. On Computer-Aided Design

2021 **DATE**, Design, Automation and Test in Europe Conference

2021 **RTAS**, IEEE Real-Time and Embedded Technology and Applications Symposium
2019– **SAMOS**, Int. Conf. Embedded Computer Systems: Architectures, Modeling And Simulation
2019– **RAPIDO**, Workshop on Rapid Simulation and Performance Evaluation: Methods and Tools
2018– **Computing Frontiers**, ACM Int. Conf. on Computing Frontiers
2017–2020 **CPSWS**, CPS Summer School and Workshop
2017– **ReCoSoC**, Int. Symp. on Reconfigurable Communication-centric Systems-on-Chip
2017– **DASIP**, Conf. on Design and Architectures for Signal and Image Processing
2017– **DCIS**, Conf. on Design of Circuits and Integrated Systems
2015 **ISCE**, IEEE Int. Symp. on Consumer Electronics
2014, 2017 **TAEE**, Tecnología, Aprendizaje y Enseñanza de la Electrónica
2013 **ISVLSI**, IEEE Computer Society Annual Symp. on VLSI
2013 **DAC**, Design Automation Conference
2011, 2012 **FPL**, Int. Conf. on Field Programmable Logic and Applications

Participation in projects (previous)

European projects **CERBERO**, Cross-layer modEl-based fRamework for multi-oBjective dEsign of Reconfigurable systems in unceRtain hybRid envirOnments (2017–2019, H2020 RIA, 4 996 460€), **HELICoiD**, HypErspectraL Imaging Cancer Detection (2014–2016, FP7 FET-Open, 992 762€), **SMART**, Secure, Mobile visual sensor networks ArchiTecture (2009–2012, ARTEMIS JTI, 276 339€),

National projects **PLATINO**, Distributed HW/SW Platform for Intelligent Processing of Heterogeneous Sensor Data in Large Open Areas Surveillance Applications (2018–2020, SP, 194 810€), **MR-UHDTV**, Mixed Reality over Ultra High Definition Television (2014–2016, SP, 80 949€), **RECINTO**, Interoperable Reconfiburability (2011, UPM/Madrid Region, 9102€), **TecnoCAI**, Efficient and intelligent technologies for health and comfort in indoor environments (2009–2012, SP, 252 000€), **DR.SIMON**, Dynamic Reconfigurability for Scalability In Multimedia Oriented Networks (2009–2011, SP, 69 800€), **ASISTENTUR**, Advanced Hardware System for Urban Environments Driving Assistance (2004–2007, SP, 88 825€)

Private funding Analysis and study of the operation of a new alarm system model (2014, Securitas Direct, 1.9k€), Analysis and behaviour characterization of the Verisure Fast II control panel (alarm system) (2013, Securitas Direct, 14.8k€), HW/HW and HW/SW integration for WSN technologies (2009, MTP-Métodos y Procesos en Ingeniería, 6k€, Health Monitoring, (2009, Airlyper, 24k€, HW/HW integration for WSN technologies (2008, MTP-Métodos y Procesos en Ingeniería, 11.6k€, WSN tool requirements (2007, MTP-Métodos y Procesos en Ingeniería, 20k€, FPGA system for the PEM Unit Tester of GAIA CRF045 and CRF046 (2007, EADS-CRISA, 27.5k€, FPGA system for GAIA CRF041_GAIA_TEST system test (2007, EADS-CRISA, 20k€, R&S's Argus driver for the control of a sub-tone decoding device, Rohde and Schwarz S.A., 2.5k€

Students supervision

Current students

PhD Thesis

2021– **Seungah Lee**, *Inria/IRISA, Univ Rennes*, co-supervised (35%) with E. Casseau (30%) and A. Kritikakou (35%)
Efficient designs of On-Board heterogeneous Embedded Systems for Space Applications

2021– **Jérémy Guillaume**, *IETR, CentraleSupélec*, co-supervised (40%) with A. Nafkha (30%) and M. Pelcat (30%)
SGaLeaks. The Screaming Gate Array: Study and characterization of IP data leakages in mixed-signal FPGA SoCs

2018– **Jaime Sancho**, *UPM*, co-supervised (50%) with E. Juárez
Automatically Accelerated Hyperspectral 3D Point Cloud Generation

Master Thesis Interns

2022 **Baili Liu**, *Student at Nantes University*
Energy-efficiency design for IoT Devices using wake-up circuits based on FPGA

Graduated students

Master Thesis

2021 **Sami Ben Ali**, *Student at National Engineering school of Tunis (ENIT) & Technical University of Braunschweig*
Side-channel attacks to AI

2020 **Abbe Ahmed Khalifa**, *Student at EURECOM*
Circuit Diversification for Improved Security of FPGA Computing Architectures

2018 **Jaime Sancho**, *UPM*
Energy and Performance Modeling of NVIDIA Jetson TX1 Embedded GPU in Hyperspectral Image Classification Tasks for Cancer detection Using Machine Learning

Engineering Thesis (equiv. MEng)

2013 **Iván Flores**, *CEI, UPM*
Implementation of evolvable hardware in a systolic array by means of virtual reconfigurable circuits

2011 **Javier Mora**, *CEI, UPM*
Implementation of evolvable hardware in a systolic array by means of partial reconfiguration

2011 **Alberto Vidal**, *CEI, UPM*
Design of an architecture for the implementation of adaptive wavelet transforms for image compression in embedded systems

2011 **Patricia Tejerina**, *CEI, UPM*
Image processing hardware system on a chip for real-time movement detection

2009 **Carlos Melchor Terleira**, *CEI, UPM*
Integration of the backpropagation algorithmn in an embedded hardware processor for on-line training

BEng Thesis

2019 **Sergio Sanchez**, *UPM, CITSEM*
Embedded GPU based Accelerator Implementation of a Support Vector Machine for Brain Tumour Detection

2018 **Adolfo Vara de Rey Suárez**, *UPM, CITSEM*
CUDA-based GPU Implementation of a Spatial-Spectral Filter for Hyperspectral Classification Maps for Brain Tumor Detection

2017 **Sergio Torres**, *UPM, CITSEM*
SDSoC-based FPGA Implementation of a Spatial-Spectral Filter for Hyperspectral Classification Maps for Brain Tumor Detection

2017 **Rubén Domingo**, *UPM, CITSEM*
OpenCL-based FPGA Implementation of a Spatial-Spectral Filter of Hyperspectral Classification Maps for Brain Tumor Detection

2016 **José Ángel Valverde**, *UPM, CITSEM*
Design based on RVC-CAL of the UCLS algorithm for abundance estimation on hyperspectral images

Undergraduate research students

2016/2017 **Guillermo Bermejo**, *UPM, CITSEM*, BEng 4th year, 240 hrs

2016/2017 **David García**, *UPM, CITSEM*, BEng 4th year, 360 hrs

2016/2017 **Sergio Sánchez**, *UPM, CITSEM*, BEng 4th year, 240 hrs

Visitors to the group

Visiting students

2022 **Yanfei Zhu**, *PhD student at Edinburgh Napier University*, supervised by Zhiyuan Tan and Chan Hwang See, Saltire Emerging Researcher Visits, SICSA (The Scottish Informatics & Computer Science Alliance). April–June 2022
Side-channel analysis of Deep Neural Networks

Publications

Articles in international journals with peer-review

[J21] M. Méndez Real and **R. Salvador**. "Physical Side-Channel Attacks on Embedded Neural Networks: A Survey". *Applied Sciences* 11(15). 2021, pp.6790. DOI: 10.3390/app11156790.

[J20] J. Sancho, P. Sutradhar, G. Rosa, M. Chavarrías, A. Perez-Nuñez, **R. Salvador**, A. Lagares, E. Juárez, and C. Sanz. "GoRG: Towards a GPU-Accelerated Multiview Hyperspectral Depth Estimation Tool for Medical Applications". *Sensors* 21(12). 2021, pp.4091. DOI: 10.3390/s21124091.

[J19] H. Fabelo, S. Ortega, A. Szolna, D. Bulters, J. F. Piñeiro, S. Kabwama, A. J-O'Shanahan, H. Bulstrode, S. Bisshopp, B. R. Kiran, D. Ravi, R. Lazcano, D. Madroñal, C. Sosa, C. Espino, M. Marquez, M. d. L. L. Plaza, R. Camacho, D. Carrera, M. Hernández, G. M. Callicó, J. Morera, B. Stanciulescu, G. Yang, **R. Salvador**, E. Juárez, C. Sanz, and R. Sarmiento. "In-Vivo Hyperspectral Human Brain Image Database for Brain Cancer Detection". *IEEE Access* 7. 2019, pp.39098–39116. DOI: 10.1109/ACCESS.2019.2904788.

[J18] R. Lazcano, D. Madroñal, H. Fabelo, S. Ortega, **R. Salvador**, G. Callico, E. Juarez, and C. Sanz. "Adaptation of an Iterative PCA to a Manycore Architecture for Hyperspectral Image Processing". *Journal of Signal Processing Systems* 91(7). May 2019, pp.1–13. DOI: 10.1007/s11265-018-1380-9.

[J17] R. Lazcano, D. Madroñal, G. Florimbi, J. Sancho, S. Sanchez, R. Leon, H. Fabelo, S. Ortega, E. Torti, **R. Salvador**, M. Marrero-Martin, F. Leporati, E. Juarez, G. M. Callico, and C. Sanz. "Parallel Implementations Assessment of a Spatial-Spectral Classifier for Hyperspectral Clinical Applications". *IEEE Access* 7. 2019, pp.152316–152333. DOI: 10.1109/ACCESS.2019.2938708.

[J16] D. Madroñal, F. Arrestier, J. Sancho, A. Morvan, R. Lazcano, K. Desnos, **R. Salvador**, D. Menard, E. Juarez, and C. Sanz. "PAPIFY: Automatic Instrumentation and Monitoring of Dynamic Dataflow Applications Based on PAPI". *IEEE Access* 7. 2019, pp.111801–111812. DOI: 10.1109/ACCESS.2019.2934223.

[J15] J. Mora, **R. Salvador**, and E. de la Torre. "On the scalability of evolvable hardware architectures: comparison of systolic array and Cartesian genetic programming". *Genetic Programming and Evolvable Machines* 20(2). June 2019, pp.155–186. DOI: 10.1007/s10710-018-9340-5.

[J14] C. Rubattu, F. Palumbo, C. Sau, **R. Salvador**, J. Sérot, K. Desnos, L. Raffo, and M. Pelcat. "Dataflow-Functional High-Level Synthesis for Coarse-Grained Reconfigurable Accelerators". *IEEE Embedded Systems Letters* 11(3). 2019, pp.69–72. DOI: 10.1109/LES.2018.2882989.

[J13] H. Fabelo, S. Ortega, R. Lazcano, D. Madroñal, G. M. Callicó, E. Juárez, **R. Salvador**, D. Bulters, H. Bulstrode, A. Szolna, J. F. Piñeiro, C. Sosa, A. J. O'Shanahan, S. Bisshopp, M. Hernández, J. Morera, D. Ravi, B. R. Kiran, A. Vega, A. Báez-Quevedo, G.-Z. Yang, B. Stanciulescu, and R. Sarmiento. "An Intraoperative Visualization System Using Hyperspectral Imaging to Aid in Brain Tumor Delineation". *Sensors* 18(2) 430. Feb. 2018, pp.1–21. DOI: 10.3390/s18020430.

[J12] H. Fabelo, S. Ortega, D. Ravi, B. R. Kiran, C. Sosa, D. Bulters, G. M. Callico, H. Bulstrode, A. Szolna, J. F. Piñeiro, S. Kabwama, D. Madroñal, R. Lazcano, A. J. O'Shanahan, S. Bisshopp, M. Hernández, A. Báez, G.-Z. Yang, B. Stanciulescu, **R. Salvador**, E. Juárez, and R. Sarmiento. "Spatio-spectral classification of hyperspectral images for brain cancer detection during surgical operations". *PLoS ONE* 13(3) e0193721. Mar. 2018, pp.1–27. DOI: 10.1371/journal.pone.0193721.

[J11] G. Florimbi, H. Fabelo, E. Torti, R. Lazcano, D. Madroñal, S. Ortega, **R. Salvador**, F. Leporati, G. Danese, A. Báez-Quevedo, G. M. Callicó, E. Juárez, C. Sanz, and R. Sarmiento. "Accelerating the K-Nearest Neighbors Filtering Algorithm to Optimize the Real-Time Classification of Human Brain Tumor in Hyperspectral Images". *Sensors* 18(7) 2314. July 2018. DOI: 10.3390/s18072314.

[J10] E. Martel, R. Lazcano, J. López, D. Madroñal, **R. Salvador**, S. López, E. Juarez, R. Guerra, C. Sanz, and R. Sarmiento. "Implementation of the Principal Component Analysis onto High-Performance Computer Facilities for Hyperspectral Dimensionality Reduction: Results and Comparisons". *Remote Sensing* 10(6) 864. June 2018. DOI: 10.3390/rs10060864.

[J9] H. Fabelo, R. Camacho, M. L. Plaza, G. M. Callico, R. Lazcano, D. Madroñal, **R. Salvador**., E. Juarez, and R. Sarmiento. "Detection of human brain cancer in pathological slides using hyperspectral images". *Neuro-Oncology* 19 suppl_3. May 2017, pp.iii37. DOI: 10.1093/neuonc/nox036.133.

[J8] R. Lazcano, D. Madroñal, **R. Salvador**, K. Desnos, M. Pelcat, R. Guerra, H. Fabelo, S. Ortega, S. Lopez, G. Callico, E. Juarez, and C. Sanz. "Porting a PCA-based hyperspectral image dimensionality reduction algorithm for brain cancer detection on a manycore architecture". *Journal of Systems Architecture* 77. June 2017, pp.101–111. DOI: 10.1016/j.sysarc.2017.05.001.

[J7] D. Madroñal, R. Lazcano, **R. Salvador**, H. Fabelo, S. Ortega, G. Callico, E. Juarez, and C. Sanz. "SVM-based real-time hyperspectral image classifier on a manycore architecture". *Journal of Systems Architecture* 80. Oct. 2017, pp.30–40. DOI: 10.1016/j.sysarc.2017.08.002.

[J6] E. Barrera, M. Ruiz, D. Sanz, J. Vega, R. Castro, E. Juárez, and **R. Salvador**. "Test bed for real-time image acquisition and processing systems based on FlexRIO, CameraLink, and EPICS". *Fusion Engineering and Design* 89(5). May 2014. Proceedings of the 9th {IAEA} Technical Meeting on Control, Data Acquisition, and Remote Participation for Fusion Research, pp.633–637. DOI: 10.1016/j.fusengdes.2014.02.010.

[J5] **R. Salvador**, A. Otero, J. Mora, E. de la Torre, T. Riesgo, and L. Sekanina. "Self-Reconfigurable Evolvable Hardware System for Adaptive Image Processing". *IEEE Transactions on Computers* 62(8). Aug. 2013, pp.1481–1493. DOI: 10.1109/TC.2013.78.

[J4] **R. Salvador**, A. Vidal, F. Moreno, T. Riesgo, and L. Sekanina. "Accelerating FPGA-based evolution of wavelet transform filters by optimized task scheduling". *Microprocessors and Microsystems* 36(5). July 2012. Special Issue on Design of Circuits and Integrated Systems, pp.427–438. DOI: 10.1016/j.micpro.2012.02.002.

[J3] **R. Salvador**, F. Moreno, T. Riesgo, and L. Sekanina. "Evolutionary Approach to Improve Wavelet Transforms for Image Compression in Embedded Systems". *EURASIP Journal on Advances in Signal Processing* 2011. Jan. 2011, pp.1–20. DOI: 10.1155/2011/973806.

[J2] F. Moreno, J. Alarcon, **R. Salvador**, and T. Riesgo. "Reconfigurable Hardware Architecture of a Shape Recognition System Based on Specialized Tiny Neural Networks With Online Training". *IEEE Transactions on Industrial Electronics* 56(8). Aug. 2009, pp.3253–3263. DOI: 10.1109/TIE.2009.2022076.

[J1] M. Ruiz, **R. Salvador**, and M. Recuero. "Implementation of Narrow-Band Algorithms according to ANSI S3.6-1996". *The Journal of the Acoustical Society of America* 110 5. Dec. 2001, pp.2681–2682. DOI: 10.1121/1.4777190.

Book chapters

[BC1] F. Moreno, I. Lopez, R. Sanz, **R. Salvador**, and J. Alarcon. "Embedded Intelligence on Chip: Some FPGA based Design Experiences". In: *Pattern Recognition Recent Advances*. Ed. by A. Herout. InTech, Feb. 2010. DOI: 10.5772/9366.

Invited talks, tutorials and seminars

[IT3] **R. Salvador**. "Reconfigurable embedded computing. Self-adaptation and high-level design techniques for signal processing applications". Presentation slides. VAADER Seminars. VAADER Seminars, IETR (Institut d'Électronique et de Télécommunications de Rennes), Rennes, France, Nov. 7, 2017. https://tinyurl.com/y7uc636b.

[IT2] **R. Salvador**, S. Ortega, D. Madroñal, H. Fabelo, R. Lazcano, G. M. Callico, E. Juarez, R. Sarmiento, and C. Sanz. *HELICoiD: Interdisciplinary and Collaborative Project for Real-time Brain Cancer Detection: Invited Paper*. ACM International Conference on Computing Frontiers. Siena, Italy, May 2017. DOI: 10.1145/3075564.3076262.

[IT1] **R. Salvador**. *Evolvable Hardware in FPGAs: Embedded Tutorial*. Invited tutorial. 2016 International Conference on Design and Technology of Integrated Systems in Nanoscale Era (DTIS). Istanbul, Turkey, Apr. 2016. DOI: 10.1109/DTIS.2016.7483877. https://tinyurl.com/y8t4rdh9.

International conferences with peer-review

[C32] J. Guillaume, M. Pelcat, A. Nafkha, and **R. Salvador**. "Virtual Triggering: a Technique to Segment Cryptographic Processes in Side-Channel Traces". In: *2022 IEEE Workshop on Signal Processing Systems (SiPS)*. 2022, pp.1–6. DOI: 10.1109/SiPS55645.2022.9919238.

[C31] M. Villa, J. Sancho, G. Vazquez, G. Rosa, G. Urbanos, A. Martin-Perez, P. Sutradhar, **R. Salvador**, M. Chavarrías, A. Lagares, E. Juárez, and C. Sanz. "Data-Type Assessment for Real-Time Hyperspectral Classification in Medical Imaging". In: *Design and Architecture for Signal and Image Processing*. 2022, pp.123–135. DOI: 10.1007/978-3-031-12748-9_10.

[C30] J. Sancho, M. Villa, G. Urbanos, M. Villanueva, P. Sutradhar, G. Rosa, A. Martin, G. Vazquez, M. Chavarrias, R. Salvador, A. Lagares, E. Juarez, and C. Sanz. "An Embedded GPU Accelerated Hyperspectral Video Classification System in Real-Time". In: *2021 XXXVI Conference on Design of Circuits and Integrated Systems (DCIS)*. 2021, pp.1–6. DOI: 10.1109/DCIS53048.2021.9666171.

[C29] J. Sancho, G. Urbanos, L. Ruiz, M. Villanueva, G. Rosa, A. Diaz, M. Villa, M. Chavarrías, A. Lagares, **R. Salvador**, E. Juárez, and C. Sanz. "Towards GPU Accelerated HyperSpectral Depth Estimation in Medical Applications". In: *XXXV Conference on Design of Circuits and Integrated Systems (DCIS)*. 2020, pp.1–6. DOI: 10.1109/DCIS51330.2020.9268649.

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